**[0065]** Some of the embodiments disclosed herein may be implemented in software, hardware, application logic, or a combination of software, hardware, and application logic. The software, application logic, and/or hardware may reside on memory **40**, the control apparatus **20**, or electronic components, for example. In some example embodiment, the application logic, software or an instruction set is maintained on any one of various conventional computer-readable media. In the context of this document, a "computer-readable medium" may be any non-transitory media that can contain, store, communicate, propagate or transport the instructions for use by or in connection with an instruction execution system, apparatus, or device, such as a computer or data processor circuitry, with examples depicted at FIGS. **9** and **10** computer-readable medium may comprise a non-transitory computer-readable storage medium that may be any media that can contain or store the instructions for use by or in connection with an instruction execution system, apparatus, or device, such as a computer.

**[0066]** Without in any way limiting the scope, interpretation, or application of the claims appearing below, a technical effect of one or more of the example embodiments disclosed herein is enabling RF power DACs to be used in user equipment and other radios, systems, and the like in which OOB noise may be kept relatively low.

**[0067]** If desired, the different functions discussed herein may be performed in a different order and/or concurrently with each other. Furthermore, if desired, one or more of the above-described functions may be optional or may be combined. Although various aspects of the invention are set out in the independent claims, other aspects of the invention comprise other combinations of features from the described embodiments and/or the dependent claims with the features of the independent claims, and not solely the combinations explicitly set out in the claims. It is also noted herein that while the above describes example embodiments, these descriptions should not be viewed in a limiting sense. Rather, there are several variations and modifications that may be made without departing from the scope of the present invention as defined in the appended claims. Other embodiments may be within the scope of the following claims. The term "based on" includes "based on at least." The use of the phase "such as" means "such as for example" unless otherwise indicated.

**1**. A method comprising:

receiving a first error signal representative of a first noise including a first quantization noise carried by a quadrature signal;

receiving a second error signal representative of a second noise including a second quantization noise carried by an in-phase signal; and

determining one or more bits in a polar domain, wherein the one or more bits cancel a portion of the first noise and the second noise represented by the first error signal and the second error signal.

**2**. The method of claim **1** further comprising:

combining, in the polar domain, the one or more bits with the amplitude signal and the phase signal to cancel the portion.

**3**. The method of claim **2**, wherein the combining comprises subtracting.

**4**. The method of claim **1** further comprising:

determining, by two sigma delta modulators from the first error signal and the second error signal, the one or more bits.

**5**. The method of claim **4**, wherein the two sigma delta modulators comprise two parallel sigma delta modulators, wherein the two parallel sigma delta modulators each have a feedback gain adaptively chosen according to at least the amplitude signal, the phase signal, and one or more signs of the two parallel sigma delta modulators outputs.

**6**. The method of claim **5** further comprising:

choosing the feedback gain proportional to a rectangular domain change equivalent of least significant bit changes of the amplitude signal and the phase signal.

**7**. The method of claim **5** further comprising:

choosing from one or more gain levels, one of the gain levels providing a high gain in the two parallel sigma delta modulators.

**8**. The method of claim **4**, wherein the two sigma delta modulators have different non-even quantizer levels, and wherein the non-even quantizer levels are adaptively chosen according to at least the amplitude signal, the phase signal, and the one or more signs of the two parallel sigma delta modulators outputs.

**9**. The method of claim **8** further comprising:

choosing the non-even quantizer levels, such that the non-even quantizer levels are proportional to rectangular domain change equivalents of one or more least significant bits changes of the amplitude signal and the phase signal.

**10**. The method of claim **1**, wherein the first and second noise is due in part to at least one of a regular or an irregular step size of quantized polar domain signals.

**11**. An apparatus comprising:

at least one processor circuitry; and

at least one memory circuitry including computer program code, the at least one memory circuitry and the computer program code configured to, with the at least one processor circuitry, cause the apparatus to perform at least the following:

receive a first error signal representative of a first noise including a first quantization noise carried by a quadrature signal;

receive a second error signal representative of a second noise including a second quantization noise carried by an in-phase signal; and

determine one or more bits in a polar domain, wherein the one or more bits cancel a portion of the first noise and the second noise represented by the first error signal and the second error signal.

**12**. The apparatus of claim **11**, wherein the apparatus is further configured to at least combine, in the polar domain, the one or more bits with the amplitude signal and the phase signal to cancel the portion.

**13**. The apparatus of claim **12**, wherein the combine comprises a subtract.

**14**. The apparatus of claim **11**, wherein the apparatus is further configured to at least determine, by two sigma delta modulators from the first error signal and the second error signal, the one or more bits.

**15**. The apparatus of claim **14**, wherein the two sigma delta modulators comprise two parallel sigma delta modulators, wherein the two parallel sigma delta modulators each have a feedback gain adaptively chosen according to at least the